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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
RICHARDS, N DREW	

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 10/05/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/758,321	SEGAWA ET AL.	
	Examiner	Art Unit	
	N. Drew Richards	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 January 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 09/518,321.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *1/15/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 14, 16, 20 and 24 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 14, 16, 20 and 24 claim a storage capacity electrode which constitute a capacitance. The claims are indefinite as it is not clear whether a capacitor is being claimed (thus, two electrodes) or whether a single electrode is being claimed that has capacitance by itself. Further, it is noted that the language of these claims is somewhat confusing as the grammar is incorrect.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1, 5, 6, 8-13 and 21-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's admitted prior art in view of Yamanaka (U.S. Patent No. 5,834,797).

Applicant's admitted prior art as discussed on pages 1-5 of the specification and shown in figures 8-10 teaches a display device in which a thin film transistor is disposed on an insulative substrate. The thin film transistor comprises:

a first gate electrode 11, a gate insulating film 12, a semiconductor film 13 formed on the gate insulating film 12 and having a channel 13c;

a insulating film 15; and

a display electrode 19 connected to a source which is formed in the semiconductor film 13, the display electrode 19 being elongated so as to extend above the channel of the thin film transistor (page 4 lines 4-8).

Applicant's admitted prior art does not teach a second gate electrode formed between the first gate electrode and the display electrode. Yamanaka teaches a thin film transistor having a channel region with a first gate electrode beneath the channel region and a second gate electrode above the channel region.

Applicant's admitted prior art and Yamanaka are combinable because they are from the same field of endeavor. At the time of the invention it would have been obvious to a person of ordinary skill in the art to form a second gate electrode above the channel region which would be between the first gate electrode and the display electrode. The motivation for doing so is to suppress a leak current between the drain and the source. Therefore, it would have been obvious to combine Applicant's admitted prior art with Yamanaka to obtain the invention of claim 1.

With regards to claims 5 and 6, figure 9 teaches a stopper insulating film 14, aplternatively a portion of layer 15 can be considered the stopper insulating film. Layer

15 is taught as being a silicon oxide, silicon nitride, silicon oxide layer so that a portion of the bottom silicon oxide is considered the stopper insulating film as required by claim 6.

With regards to claims 8 and 9, the first gate electrode is a double gate structured electrode divided above the channel as seen in figure 9, and the second gate electrode from Yamanaka would be a double gate structured electrode divided corresponding to the first gate electrode so as to produce the same suppressed leak current between the source and drain in the area above both first gate electrodes.

With regard to claim 10, the display electrode is a reflective display electrode made of a reflective material.

With regard to claim 11, it would have been obvious to one of ordinary skill in the art at the time of the invention to form the reflective display electrode of Al-Nd alloy as Al and Nd are well known electrode materials commonly used in the art as reflective electrodes.

With regard to claim 12, the display electrode is an electrode used in a liquid display device.

With regard to claim 13, the device of the admitted prior art further teaches a light emitting layer 21 formed on the display electrode 19. The limitation of the display electrode used in an organic electroluminescent device is merely an intended use limitation that does not structurally distinguish over the prior art. The display electrode 19 is capable of being used in an organic electroluminescent device and thus reads on the claim. Further, even if the limitation is taken as further limiting the structure, the

limitation is considered obvious to one of ordinary skill in the art. One of ordinary skill in the art would recognize the well known use of thin film transistors with reflective electrodes in organic electroluminescent devices and would therefore been motivated to use the device as claimed in an organic electroluminescent device instead of the liquid display device of the Admitted prior art.

With regard to claim 21, Applicant's admitted prior art as discussed on pages 1-5 of the specification and shown in figures 8-10 teaches a display device comprising:

an insulative substrate 10;

a thin film transistor including a first gate electrode 11, a gate insulating film 12, and a channel region 13c;

a display electrode 19 connected to a source which is formed in the semiconductor film 13, the display electrode 19 being elongated so as to extend above the channel of the thin film transistor (page 4 lines 4-8).

Applicant's admitted prior art does not teach an electrode provided between the channel region and the display electrode. Yamanaka teaches a thin film transistor having a channel region with a first gate electrode beneath the channel region and a second gate electrode above the channel region. In combination, Yamanaka's second gate electrode would be between the channel region and the display electrode of the admitted prior art. The limitation of a gate voltage being applied to the electrode is merely an intended use limitation that does not structurally distinguish over the prior art.

The electrode is capable of having a gate voltage applied to it and thus reads on the limitation.

Applicant's admitted prior art and Yamanaka are combinable because they are from the same field of endeavor. At the time of the invention it would have been obvious to a person of ordinary skill in the art to form a second gate electrode above the channel region which would be between the channel region and the display electrode. The motivation for doing so is to suppress a leak current between the drain and the source. Therefore, it would have been obvious to combine Applicant's admitted prior art with Yamanaka to obtain the invention of claim 21.

With regard to claim 22, the display electrode is a reflective display electrode made of a reflective material.

With regard to claim 23, the device of the admitted prior art further teaches a light emitting layer 21 formed on the display electrode 19. The limitation of the display electrode used in an organic electroluminescent device is merely an intended use limitation that does not structurally distinguish over the prior art. The display electrode 19 is capable of being used in an organic electroluminescent device and thus reads on the claim. Further, even if the limitation is taken as further limiting the structure, the limitation is considered obvious to one of ordinary skill in the art. One of ordinary skill in the art would recognize the well known use of thin film transistors with reflective electrodes in organic electroluminescent devices and would therefore been motivated to use the device as claimed in an organic electroluminescent device instead of the liquid display device of the Admitted prior art.

5. Claims 2-4, 15 and 17-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's admitted prior art in view of Vu et al. (U.S. Patent No. 5,702,963).

With regard to claim 2, Applicant's admitted prior art teaches a display device in which a thin film transistor is disposed on an insulative substrate, the thin film transistor comprising a first gate electrode 11, a gate insulating film12, a semiconductor film 13 formed on the gate insulating film and having a channel, an insulating film 15, and a display electrode 19 connected to the source. As discussed on page 4 lines 4-8, the display electrode is elongated so as to extend above the channel of the thin film transistor. Applicant's admitted prior art does not teach a second gate electrode formed between the first gate electrode and the display electrode. Vu et al. teach a thin film transistor having a channel region with a first gate electrode beneath the channel region and a second gate electrode above the channel region where the second gate electrode is connected with the first gate electrode in figure 15g, for example.

Applicant's admitted prior art and Vu et al. are combinable because they are from the same field of endeavor. At the time of the invention it would have been obvious to a person of ordinary skill in the art to use the thin film transistor of Vu et al. which forms a second gate electrode above the channel region which would be between the first gate electrode and the display electrode. The motivation for doing so is to allow

for high density circuitry in small areas. Therefore, it would have been obvious to combine Applicant's admitted prior art with Vu et al. to obtain the invention of claim 2.

With regard to claim 3, the second gate electrode is formed to be faced with the first gate electrode through the insulating film as seen in figure 15g.

With regards to claim 4, the display electrode when extended to cover the channel of the thin film transistor is rectangular. Figure 8 shows the display electrode that is not extended but it can readily be seen in the view of figure 8 that in the case where the display electrode is extended it has a rectangular shape.

With regard to claim 15, the device of the admitted prior art further teaches a light emitting layer 21 formed on the display electrode 19. The limitation of the display electrode used in an organic electroluminescent device is merely an intended use limitation that does not structurally distinguish over the prior art. The display electrode 19 is capable of being used in an organic electroluminescent device and thus reads on the claim. Further, even if the limitation is taken as further limiting the structure, the limitation is considered obvious to one of ordinary skill in the art. One of ordinary skill in the art would recognize the well known use of thin film transistors with reflective electrodes in organic electroluminescent devices and would therefore been motivated to use the device as claimed in an organic electroluminescent device instead of the liquid display device of the Admitted prior art.

With regard to claim 17, Applicant's admitted prior art teaches a display device comprising an insulative substrate 10, a thin film transistor including a gate electrode 11, a gate insulating film 12, and a channel region 13c. The device also includes a

display electrode 19 connected to the source of the thin film transistor. As discussed on page 4 lines 4-8, the display electrode is elongated so as to extend above the channel of the thin film transistor. Applicant's admitted prior art does not teach an electrode provided between the channel region of the thin film transistor and the display electrode. Vu et al. teach a thin film transistor having a channel region with a first gate electrode beneath the channel region and an electrode above the channel region where the electrode is connected with the first gate electrode in figure 15g, for example.

Applicant's admitted prior art and Vu et al. are combinable because they are from the same field of endeavor. At the time of the invention it would have been obvious to a person of ordinary skill in the art to use the thin film transistor of Vu et al. which forms an electrode above the channel region which would be between the first gate electrode and the display electrode. The motivation for doing so is to allow for high density circuitry in small areas. Therefore, it would have been obvious to combine Applicant's admitted prior art with Vu et al. to obtain the invention of claim 17.

With regard to claim 18, the display electrode is a reflective display electrode made of a reflective material.

With regard to claim 19, the device of the admitted prior art further teaches a light emitting layer 21 formed on the display electrode 19. The limitation of the display electrode used in an organic electroluminescent device is merely an intended use limitation that does not structurally distinguish over the prior art. The display electrode 19 is capable of being used in an organic electroluminescent device and thus reads on the claim. Further, even if the limitation is taken as further limiting the structure, the

limitation is considered obvious to one of ordinary skill in the art. One of ordinary skill in the art would recognize the well known use of thin film transistors with reflective electrodes in organic electroluminescent devices and would therefore been motivated to use the device as claimed in an organic electroluminescent device instead of the liquid display device of the Admitted prior art.

6. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's admitted prior art with Yamanaka (U.S. Patent No. 5,834,797) as applied to claims 1, 5, 6, 8-13 and 21-23 above, and further in view of Kim et al. (U.S. Patent No. 6100954).

Applicant's admitted prior art does not teach the stopped insulating film made of a two-layered film of SiN and organic film. Kim et al. teach a thin film transistor used in a liquid crystal display device. Kim et al. Teach on column 18 lines 51-60 forming a gate insulation film of an organic material and a layer of silicon nitride. Combined with applicant's admitted prior art, the organic material and silicon nitride would be formed in place of layer 14 as an insulator between gate 70 and the channel region.

Applicant's admitted prior art and Kim et al. are combinable because they are from the same field of endeavor. At the time of the invention it would have been obvious to a person of ordinary skill in the art to form an insulation film between the gate and the channel of an organic layer and a silicon nitride layer. The motivation for doing so is to provide a transistor free from problems such as electron trapping. Therefore, it

would have been obvious to combine Applicant's admitted prior art with Kim et al. to obtain the invention of claim 7.

7. Claims 14 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's admitted prior art with Yamanaka (U.S. Patent No. 5,834,797) as applied to claims 1, 5, 6, 8-13 and 21-23 above, and further in view of Sato et al. (U.S. Patent No. 5251049).

Applicant's admitted prior art with Yamanaka do not teach a storage capacity electrode which constitutes a capacitance where one side of the electrode is made of the same material as the first electrode.

Sato et al. teaches a thin film transistor in a pixel for a display device. Sato et al. teach a storage capacity electrode 48 made of the same material (polysilicon) as the first gate electrode.

Applicant's admitted prior art with Yamanaka and Sato et al. are combinable because they are from the same field of endeavor. At the time of the invention it would have been obvious to a person of ordinary skill in the art to form capacity storage electrode as taught by Sato et al. The motivation for doing so is to provide charge storage in each pixel. Therefore, it would have been obvious to combine Applicant's admitted prior art and Yamanaka with Sato et al. to obtain the invention of claims 14 and 24.

8. Claims 16 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's admitted prior art with Vu et al. (U.S. Patent No. 5,702,963) as applied to claims 2-4, 15 and 17-19 above, and further in view of Sato et al. (U.S. Patent No. 5251049).

Applicant's admitted prior art with Vu et al. do not teach a storage capacity electrode which constitutes a capacitance where one side of the electrode is made of the same material as the first electrode.

Sato et al. teaches a thin film transistor in a pixel for a display device. Sato et al. teach a storage capacity electrode 48 made of the same material (polysilicon) as the first gate electrode.

Applicant's admitted prior art with Vu et al. and Sato et al. are combinable because they are from the same field of endeavor. At the time of the invention it would have been obvious to a person of ordinary skill in the art to form capacity storage electrode as taught by Sato et al. The motivation for doing so is to provide charge storage in each pixel. Therefore, it would have been obvious to combine Applicant's admitted prior art and Vu et al. with Sato et al. to obtain the invention of claims 16 and 20.

Double Patenting

9. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent

and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

10. Claims 1-24 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-24 of U.S. Patent No. 6,724,011 B2. Although the conflicting claims are not identical, they are not patentably distinct from each other because claims 1-13, 15, 17-19 and 21-23 of the instant application are merely broader in scope than those of the '011 Patent and thus are anticipated by the claims of the patent. Claims 14, 16, 20 and 24 would have been obvious to one of ordinary skill in the art at the time of the invention in view of claims 1-24 of the patent in view of Sato et al. as applied above.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to N. Drew Richards whose telephone number is (571) 272-1736. The examiner can normally be reached on Monday-Friday 9:00-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (571) 272-1664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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